15W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter

- VIN Input Voltage Range: 4.2V-20V
- PVIN Input Voltage Range: 1V-20V
- Up to 15W Power Transfer
- Integrated Full-Bridge Power Stage with 17.5-m Rdson of Power MOSFETs
- Integrated 5V-100mA LDO
- Optimized for EMI Reduction
- Build

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5V

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
Revision 1.0: Production
Revision 1.1: Update EC
Revision 1.2: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE

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(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63142 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63142. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

V_{PVIN1}=V_{PVIN2}=12V, VDD=5V, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT

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V_{ISNS2}	Voltage with 1A input current	I_{PVIN}=1A, Tj=25	1.568	1.6	1.632	V
Protection						
T_{SD}	Thermal shutdown threshold	T_J rising		155		°C

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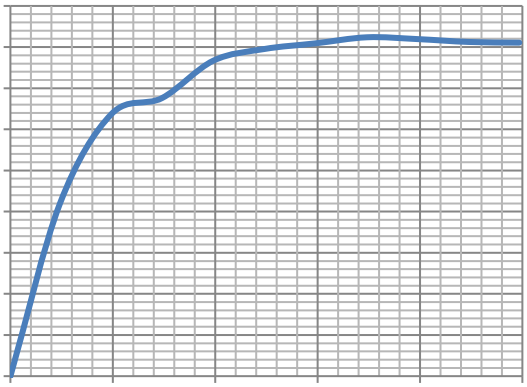

Figure 2. Transfer Efficiency with 5W RX@ Vout=5V

Figure 3. Transfer Efficiency with 10W RX@ Vout=9V

Figure 4. Transfer Efficiency with 15W RX@ Vout=12V

Figure 5. 5V LDO Iout vs Vout

Figure 6. 3.3V LDO Iout vs Vout

Figure 7. Current Sense Output Voltage vs Iin

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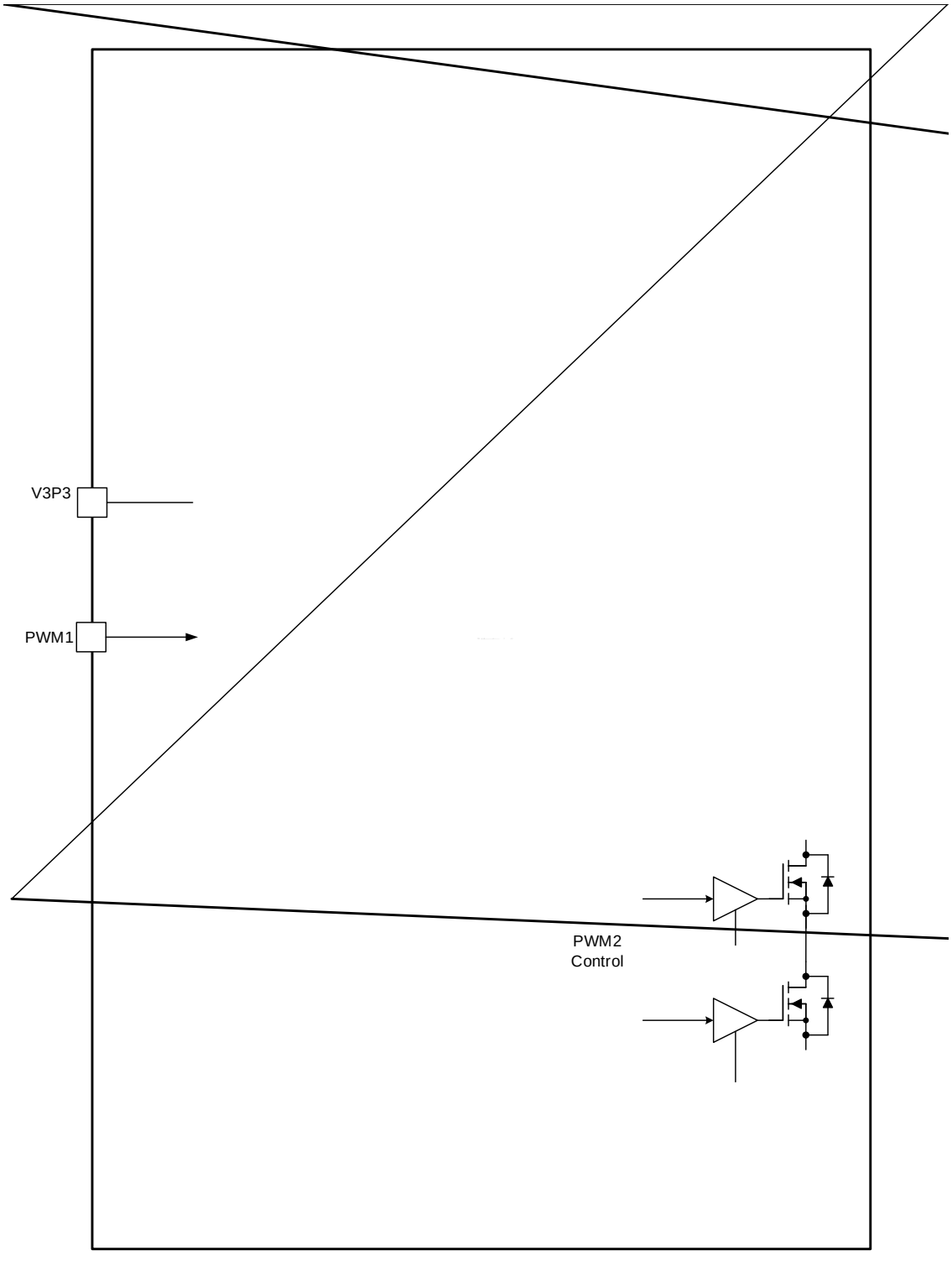

V

Figure 8. Functional Block Diagram

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3.3V LDO

The SCT63142 has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 3.3V voltage on V3V pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of MCU directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the V3V pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Q Factor Detection

The SCT63142 integrated a low cost, reliable Q factor detection circuit to assure foreign objects detection before the selection phase. It generates a small pulse to detect any foreign object on the transmitter coil, it can detect metal on the transmitter coil easily.

After chip enable, apply a low voltage level pulse to EN pin can trigger the Q factor detection feature. The pulse width should be longer than 50us but less than 200us. SW1 will be preset to 2V for 4.7ms and then pull low to ground and this apply power to LC resonant loop and Vcoil will appear damping oscillation after SW1 short to ground. The SCT63142 will generate a pulse on VDMO pin and MCU can capture this pulse to calculate the Q factor by the pulse width as the Equation 4 shows. PWM1 and PWM2 should be low in Q factor detection phase.

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Thermal Shutdown

The SCT63142 protects the device from the damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 155C, the thermal sensing circuit stops two LDOs and full bridge of 4-MOSFETs' working. When the junction temperature falls below 120C, then the device restarts.

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Typical Application

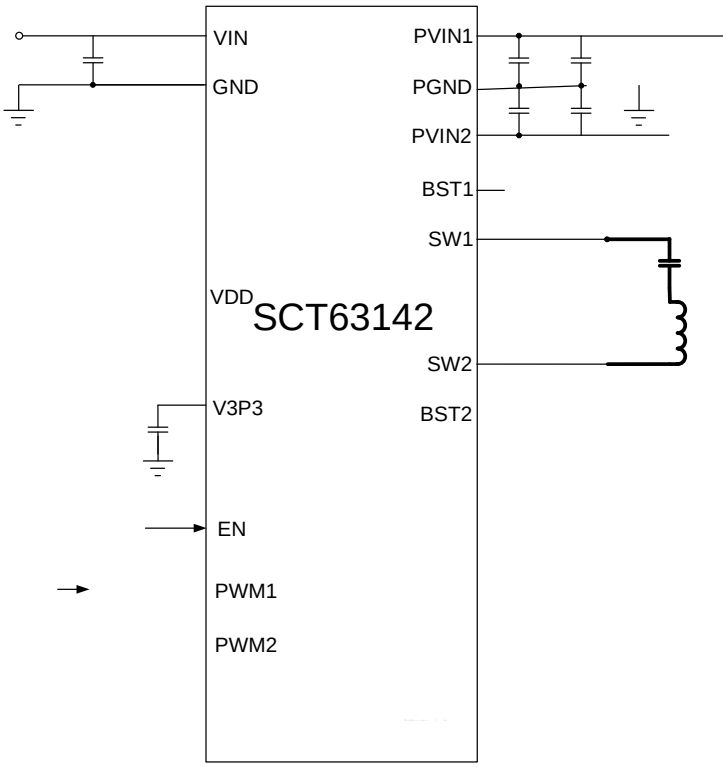

Figure 11. Same Input to VIN and PVIN

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Application Waveforms

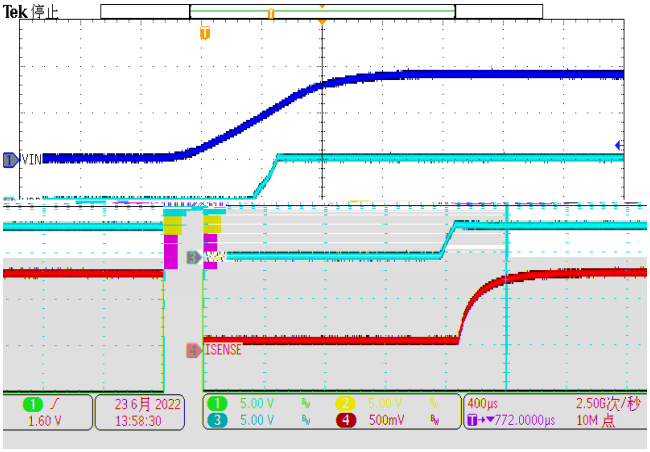

Figure 12. Power Up

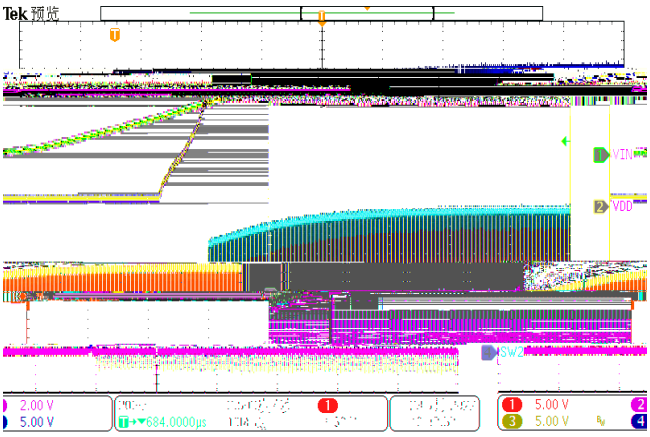

Figure 13. Power Up

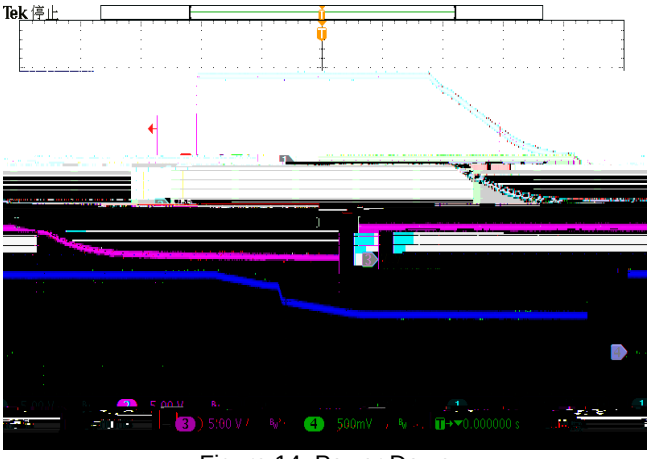

Figure 14. Power Down

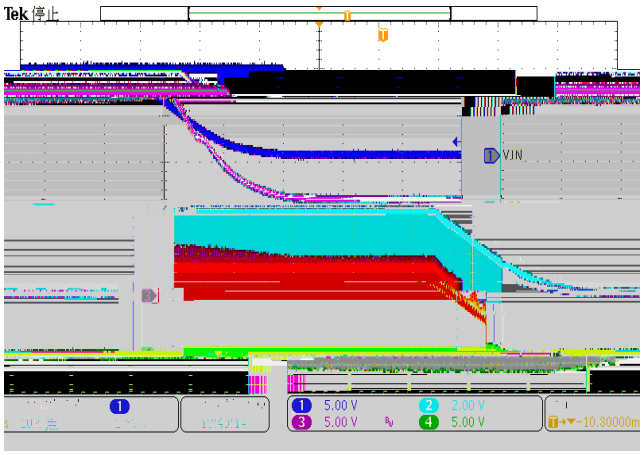

Figure 15. Power Down

Figure 16. Full bridge @Vin=9V, RX=10W

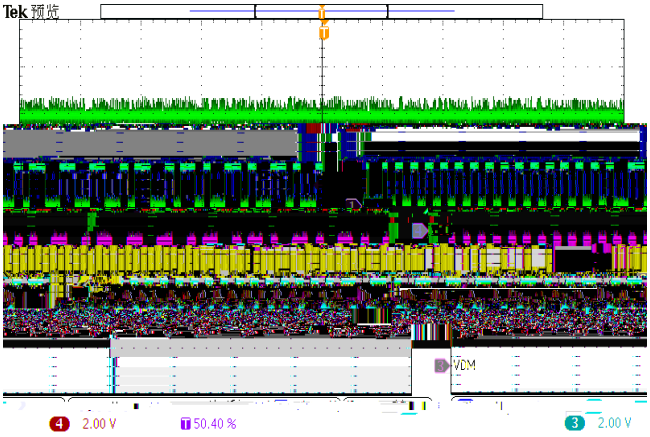

Figure 17. VDMO IDMO Demodulation Output

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Layout Guideline

Proper PCB layout is a critical for SCT63142 For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND shoulND soesi PG1sND s24(e(D)-6u)5(s)-n (s)-5(s)-14(ap)(ow)-3(ase (s)-5(s)-)-(

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FCQFN-19L (3x3) Package Outline Dimensions

		Symbol	Dimensions in Millimeters		
			Min.	Nom.	Max.
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	3.00 BSC		
	Y	E	3.00 BSC		
LEAD PITCH		e			

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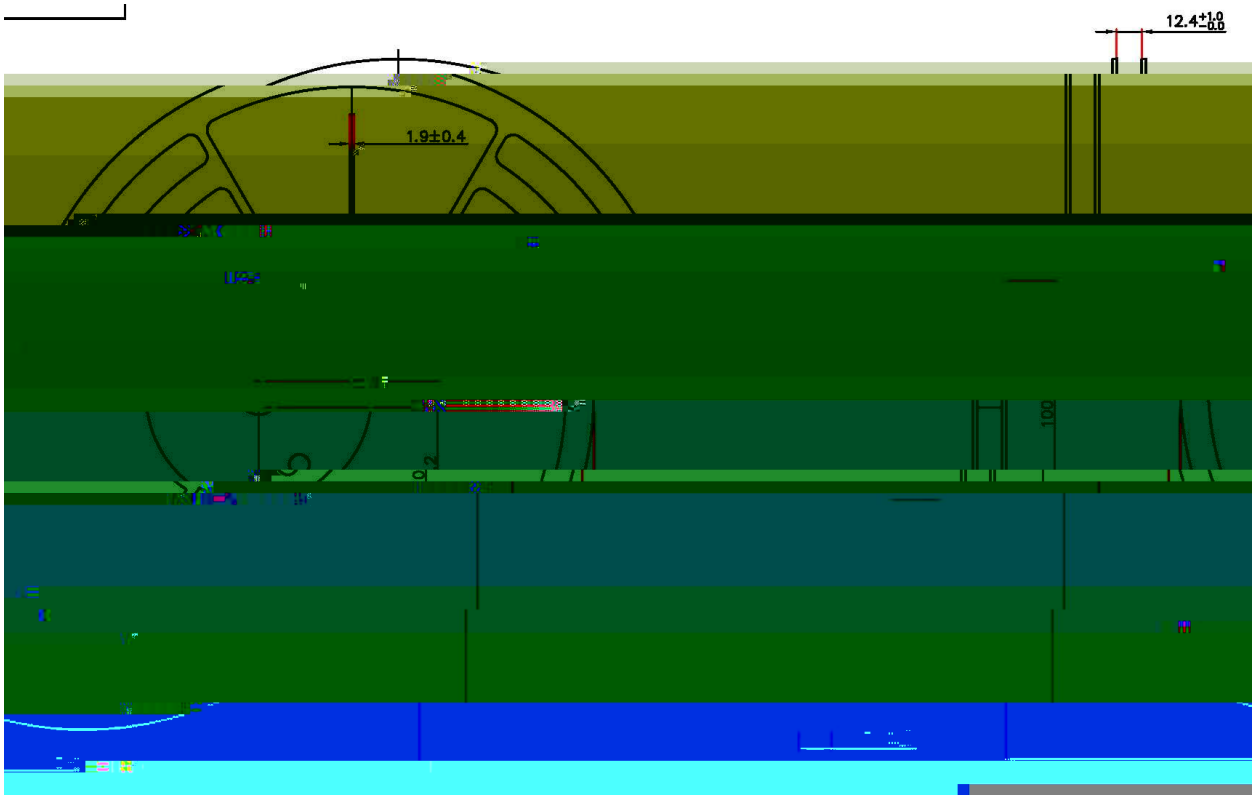

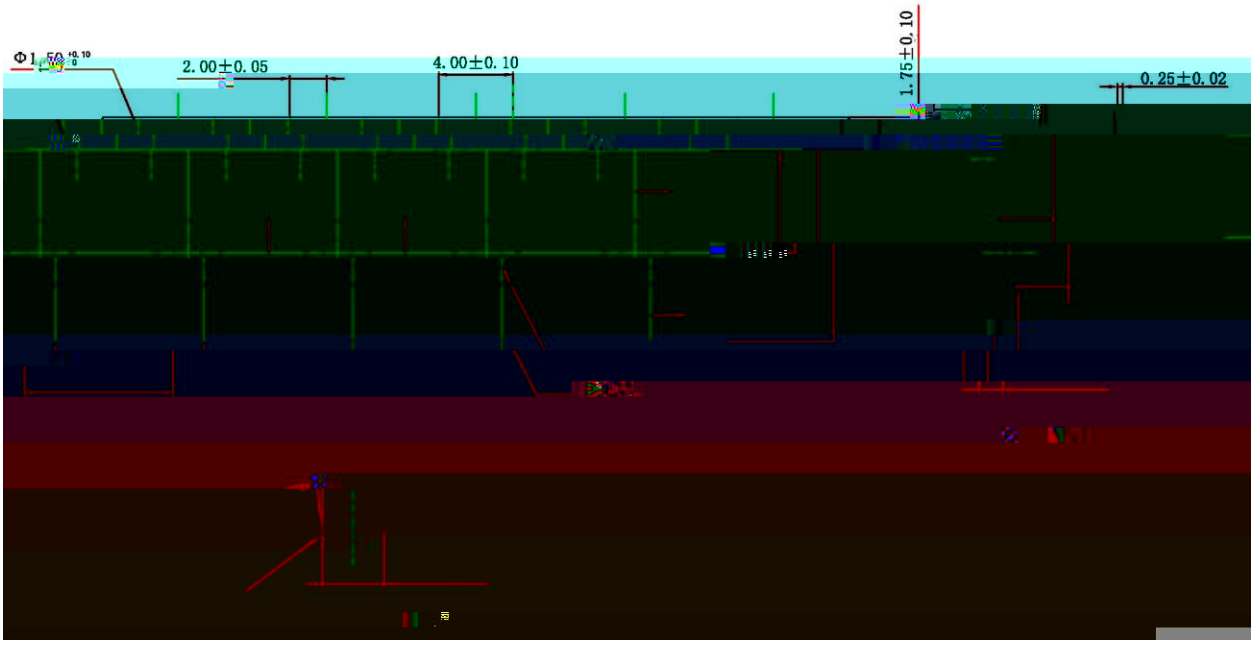

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