# 3.6V-36V Vin, 3A, High Efficiency Synchronous Step-down DCDC Converter

- Wide Input Range: 3.6V-36V
- Up to 3A Continuous Output Current
- 0.8V Feedback Reference Voltage
- Integrated 60mΩ High-Side and 36mΩ Low-Side Power MOSFETs
- Pulse Skipping Mode (PSM) with 30uA Quiescent Current in Sleep Mode
- 60ns Minimum On-time
- 4ms Internal Soft-start Time
- Adjustable Switching Frequency: 200k~2.2MHz
- Frequency Spread Spectrum (FSS) Modulation for EMI Reduction
- Precision Enable Threshold for adjustable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Parallel input path to minimize switch node ringing
- Low Dropout Mode Operation
- Over-voltage and Over-Temperature Protection
- Available in 2mm*3mm QFN-12L Package

- Battery Pack Powered System
- USB Type-C Power Delivery, USB Charging
- Industrial and Medical Distributed Power Supplies

The SCT2434D is 3A synchronous buck converters with wide input voltage, ranging from 3.6V to 36V, which integrates a 60mΩ high-side MOSFET and a 36mΩ low-side MOSFET. The SCT2434D, adopting

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| | | |
|---|---|---|
| PG | 8 | Open-drain power-good status output. Pull this pin up to a suitable voltage supply through a current limiting resistor. High = power OK, low = fault. PG output goes low when EN =low, VIN > 1V. |
| EN | 9 | Enable pin to regulator with internal pull-up current source. Pull below 1.12V to disable the converter. Float or connect to VIN to enable the converter. The t9 |

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$V_{IN}$=24V, $T_J$=-40°C~125°C, typical val ₴ ⊁ ⌋

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| | | | | |
|---|---|---|---|---|
| $t_{PGDFLT(rise}$ | Delay time to PGOOD high signal | | 2 3.5 | ms |
| $t_{PGDFLT(fall}$ | Glitch filter time constant for PGOOD function | | 130 | us |

| | | | | |
|---|---|---|---|---|
| $V_{OVP}$ | Feedback overvoltage with respect to reference voltage | $V_{FB}/V_{REF}$ rising | 110 | % |
| | | $V_{FB}/V_{REF}$ falling | 105 | % |
| $V_{BOOTUV}$ | | BOOT-SW falling | 2.7 | V |
| | | Hysteresis | 400 | mV |
| $T_{SD}$ | Thermal shutdown threshold* | $T_J$ rising | 160 | °C |
| | | Hysteresis | 20 | °C |

*Derived from bench characterization


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Figure 2. Efficiency, $F_{SW}$=400kHz, $V_{OUT}$=5V

Figure 3. Efficiency, $F_{SW}$=2.2MHz, $V_{OUT}$=5V

Figure 4. Line Regulation (FSW=400kHz,$V_{OUT}$=5V)

Figure 5. Input Current ($V_{OUT}$=5V, $I_{LOAD}$=0A)

Figure 6. Load Regulation ($V_{IN}$=12V, $V_{OUT}$=5V)

Figure 7

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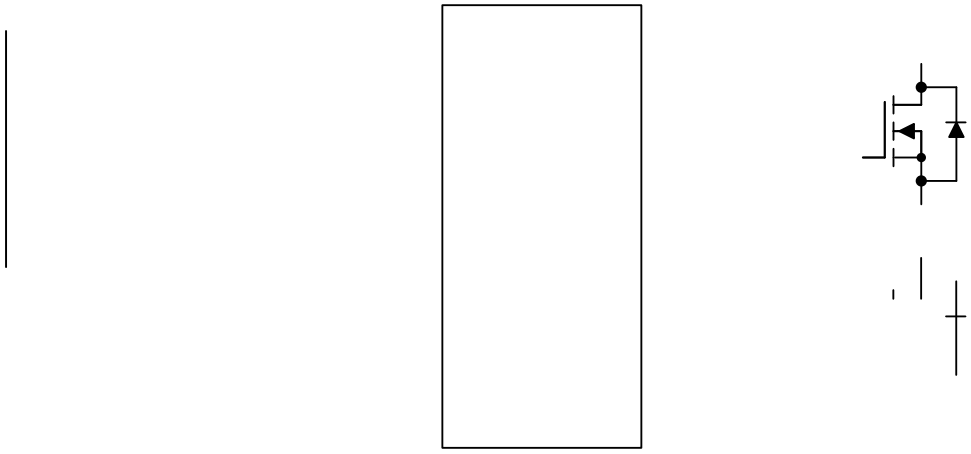

Figure 8. Functional Block Diagram

The SCT2434D is a 3.6V-36V input, 3A output, EMI friendly synchronous buck converter with built-in 60mΩ Rdson high-side and 36

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| | |
|---|---|
| 200 KHz | 182 KΩ |
| 300 KHz | 120 KΩ |
| 355 KHz | 100 KΩ |
| 400 KHz | 88.7 KΩ |
| 450 KHz | 80.6 KΩ |
| 520 KHz | 68.1 KΩ |
| 600 KHz | 59 KΩ |
| 700 KHz | 51.1 KΩ |

| | |
|---|---|
| 850 KHz | 40.2 KΩ |
| 1000 KHz | 34.8 KΩ |
| 1150 KHz | 30.1 KΩ |
| 1450 KHz | |

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Figure 10. LDO Operation Characteristic ($V_{OUT}$=5V)

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2434D implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage

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(6)

where:

$V_{rise}$ is rising threshold of Vin UVLO

$V_{fall}$ is falling threshold of Vin UVLO

$I_1$=1uA, $I_2$=3.8uA, $V_{ENR}$=1.24V, $V_{ENF}$=1.12V

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and

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$I_{LPP}$ is the inductor peak-to-peak current
$I_{LRMS}$ is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 4.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 4.5A. Because of the maximum $I_{LPEAK}$ limited

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The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor  like

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$V_{IN}$=12V, $V_{OUT}$=5V, unless otherwise noted

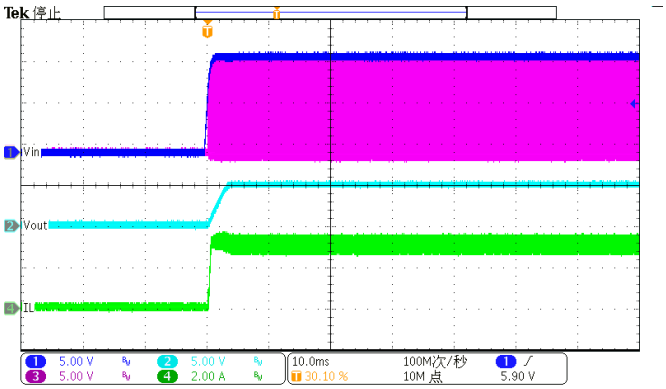


Figure 12. Power up($I_{LOAD}$=3A)

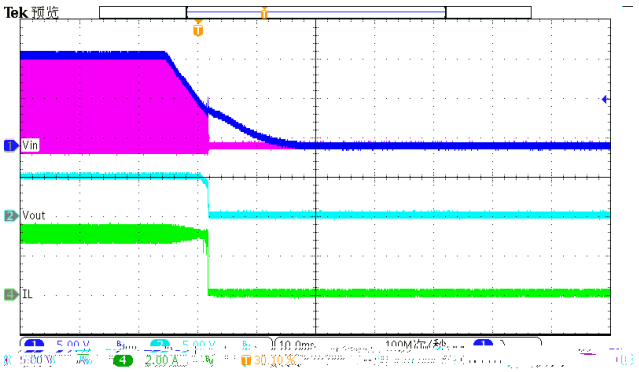


Figure 13. Power down($I_{LOAD}$=3A)

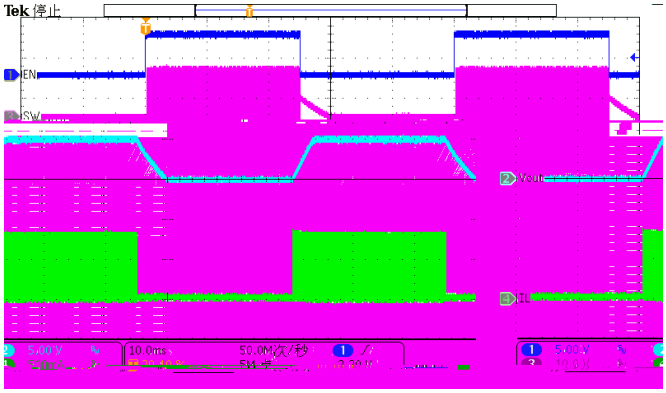


Figure 14. EN toggle ($I_{LOAD}$=0.1A)

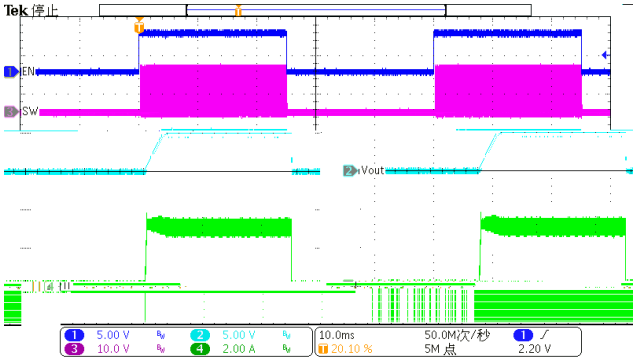


Figure 15. EN toggle ($I_{LOAD}$=3A)

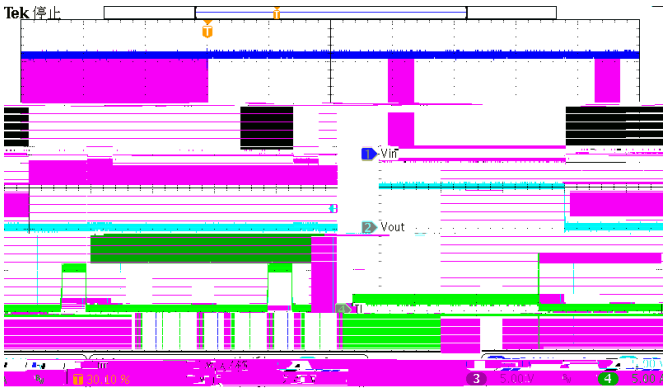


Figure 16. Over Current Protection(1A to hard short)

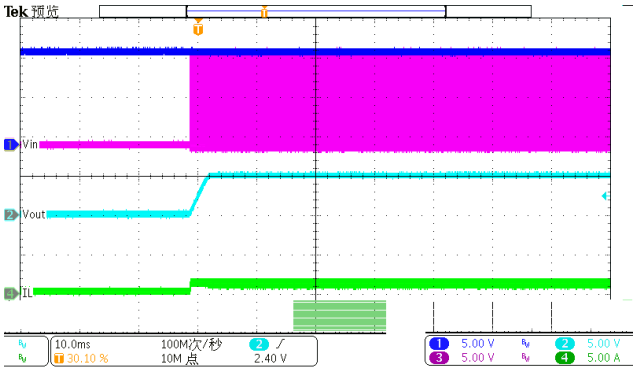


Figure 17. Over Current Release (hard short to 1A)

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Proper PCB layout is a critical for SCT2434D's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing

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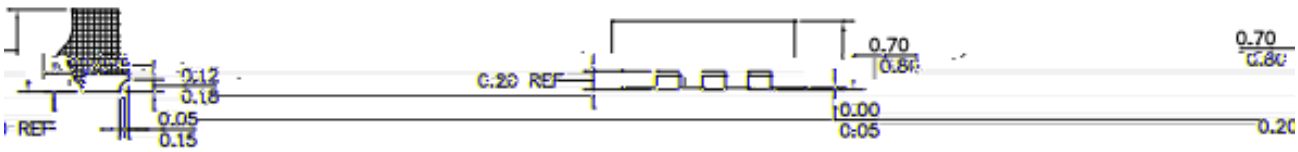
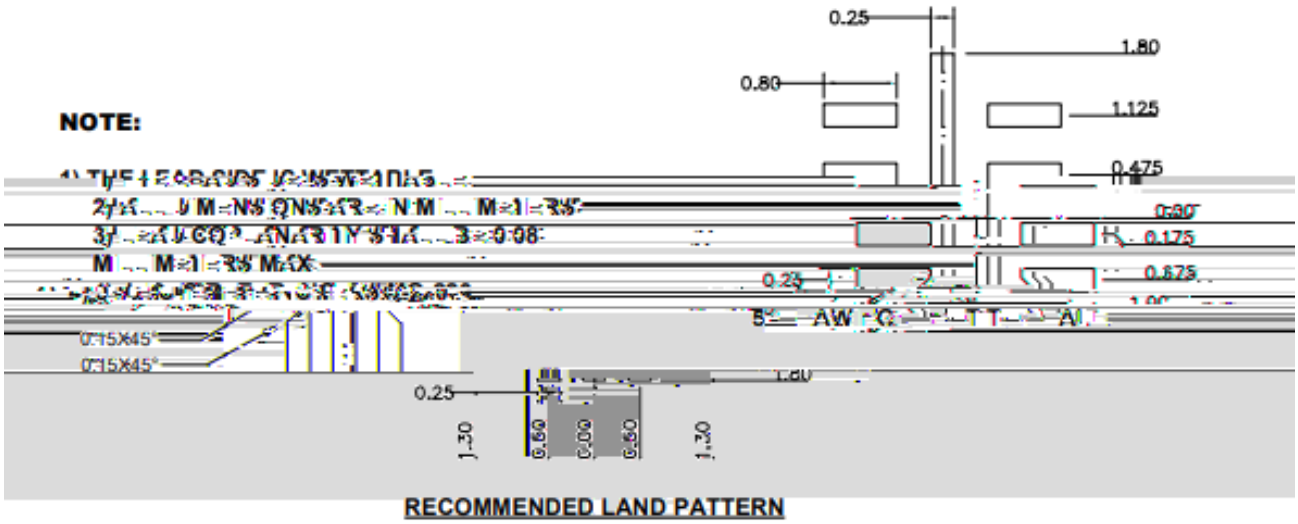
BOTTOM VIEW TOP VIEW

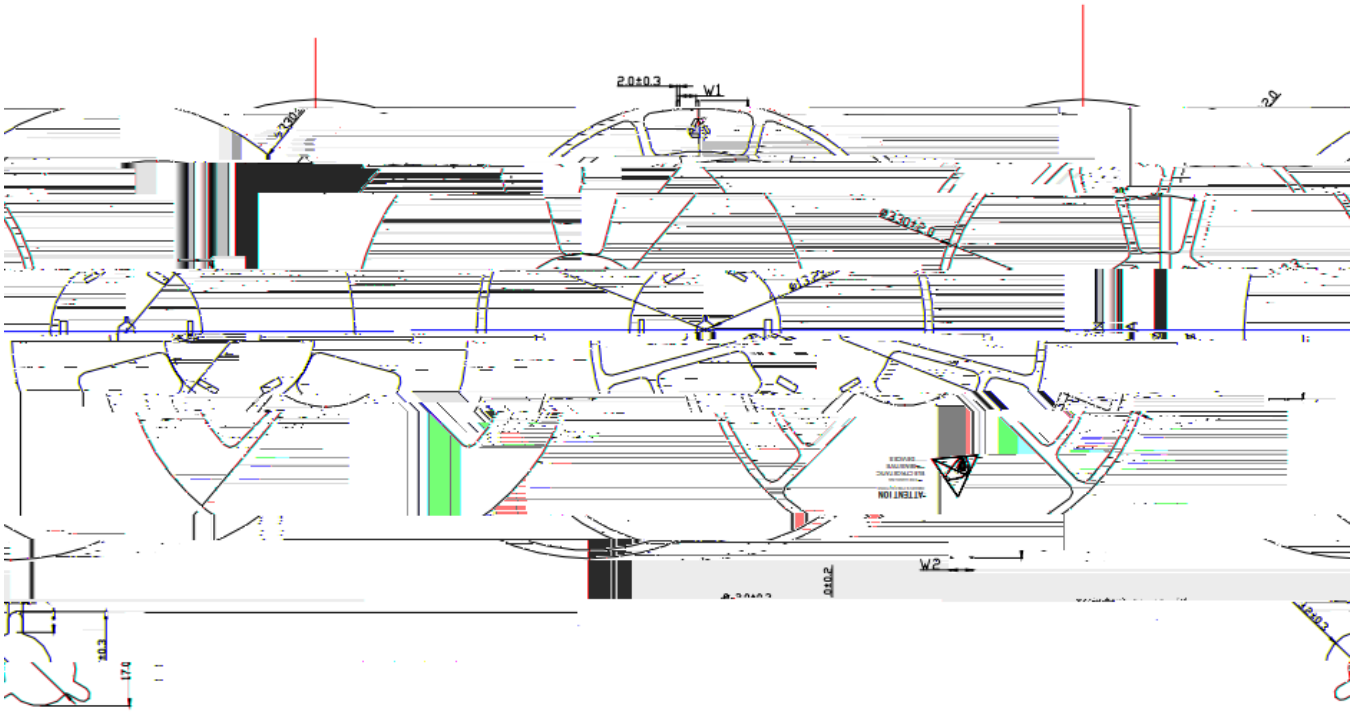


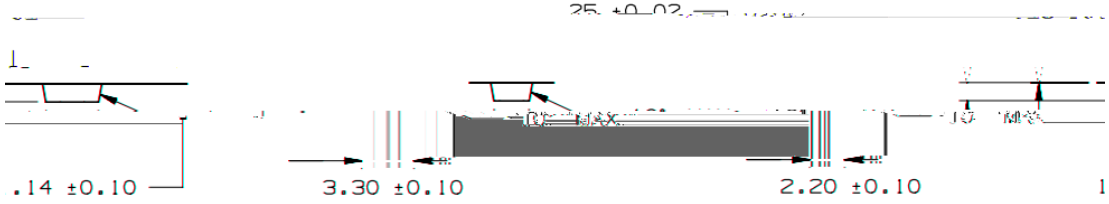

SECTION A-A SIDE VIEW




**NOTE:**

RECOMMENDED LAND PATTERN

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